WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first isolation layer on the semiconductor substrate;

a second isolation layer on the semiconductor substrate, wherein the second isolation layer is spaced apart from the first isolation layer to define a first active region therebetween;

a third isolation layer on the semiconductor substrate, wherein the third isolation layer is spaced apart from the second isolation layer to define a second active region therebetween, and wherein the first, second and third isolation layers define a row;

a first cell gate on the first active region, the first cell gate comprising a first gate dielectric layer, a first storage node, a first multiple tunnel junction barrier and a first source layer that are sequentially stacked;

a second cell gate on the second active region, the second cell gate comprising a second gate dielectric layer, a second storage node, a second multiple tunnel junction barrier and a second source layer that are sequentially stacked;

a first control line surrounding at least a portion of each sidewall of the first cell gate;

a second control line surrounding at least a portion of each sidewall of the second cell gate, the second control line disposed parallel to the first control line;

a first dielectric layer interposed between the first control line and the sidewalls of the first cell gate;

a second dielectric layer interposed between the second control line and the sidewalls of the second cell gate; and

a data line connecting to the first and second cell gates.

2. The semiconductor device of Claim 1, wherein a first side of the first cell gate overlaps a portion of the first isolation layer and a second side of the first cell gate overlaps a portion of the second isolation layer, and wherein a first side of the second cell gate overlaps a portion of the second isolation layer and a second side of the second cell gate overlaps a portion of the third isolation layer.

3. The semiconductor device of Claim 1, further comprising a fourth isolation layer and a fifth isolation layer on the semiconductor substrate, wherein the fourth isolation layer and the fifth isolation layer are parallel to the row defined by the first, second and third isolation layers and wherein the first, second and third isolation layers are positioned between the fourth isolation layer and the fifth isolation layer.

4. The semiconductor device of Claim 3, wherein the first control line and the second control line cross over the fourth isolation layer and the fifth isolation layer and wherein the data line crosses over the first, second and third isolation layers.

5. The semiconductor device of Claim 1, further comprising a first spacer interposed at least partially between the first dielectric layer and the first control line and a second spacer interposed at least partially between the second dielectric layer and the second control line.

6. The semiconductor device of Claim 5, wherein the first spacer and the second spacer comprise polysilicon spacers.

7. The semiconductor device of Claim 1, wherein a top surface of the first control line is lower than a top surface of the first source layer and wherein a top surface of the second control line is lower than a top surface of the second source layer.

8. The semiconductor device of Claim 1, further comprising a third dielectric layer between the data line and the top surface of the first and second control lines.

9. The semiconductor device of Claim 1, wherein a top surface of the first control line is higher than a top surface of the first source layer and wherein a top surface of the second control line is higher than a top surface of the second source layer, and wherein the device further comprises an insulation spacer between the first and second control lines and the data line.

10. The semiconductor device of Claim 9, wherein the insulation spacer is formed of one material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride and aluminum oxide.

11. The semiconductor device of Claim 5, further comprising a low-concentration impurity-doped region in the semiconductor substrate under both the first spacer and the second spacer and a high-concentration impurity-doped region in the semiconductor substrate under both the first control line and the second control line.

12. A semiconductor device comprising:

a semiconductor substrate;

a plurality of parallel, spaced apart first isolation layers on the semiconductor substrate;

a plurality of second isolation layers interposed between adjacent ones of the plurality of first isolation layers;

a plurality of rows of cell gates, wherein the rows of cell gates are perpendicular to the plurality of first isolation layers, and wherein each cell gate in the rows of cell gates is on at least a portion of two of the plurality of second isolation layers;

at least one dielectric layer on the sidewalls of the cell gates in the plurality of rows of cell gates;

a plurality of parallel control lines that cross over the plurality of first isolation layers, wherein each of the plurality of control lines surrounds the dielectric layer that is on the sidewalls of each cell gate in a row of the rows of cell gates that corresponds to the control line; and

a plurality of data lines that are parallel to the plurality of first isolation layers, wherein each of the plurality of data lines connects to a subset of the plurality of cell gates.

13. The semiconductor device of Claim 12, wherein each cell gates comprises a gate dielectric layer, a storage node, a multiple tunnel junction barrier and a source layer that are sequentially stacked.

14. The semiconductor device of Claim 13, wherein the data lines connect to a top surface of the cell gates.

15. The semiconductor device of Claim 12, further comprising a peripheral circuit region in the semiconductor substrate, the peripheral circuit region comprising:

a third isolation layer defining an active region in the semiconductor substrate;

a peripheral gate on the active region and on a portion of the third isolation layer; and

a peripheral gate contact plug electrically connecting to the peripheral gate.

16. The semiconductor device of Claim 15, wherein the peripheral gate comprises a gate dielectric layer, a storage node, a multiple tunnel junction barrier and a source layer sequentially stacked on the semiconductor substrate.

17. The semiconductor device of Claim 15, wherein the peripheral gate contact plug is directly connected to the storage node.

18. A method of fabricating a semiconductor device, comprising:

forming a first field isolation layer, a second field isolation layer and a third field isolation layer on a semiconductor substrate, the first and second field isolation layers defining a first active region therebetween and the second and third field isolation layers defining a second active region therebetween;

sequentially forming a gate dielectric layer, a storage node layer, a multiple tunnel junction barrier layer and a source layer on the semiconductor substrate;

patterning the source layer, the multiple tunnel junction barrier layer, the storage node layer and the gate dielectric layer to form a first cell gate and a second cell gate, the first and second cell gates each having a gate dielectric region, a storage node, a multiple tunnel junction barrier and a source region that are sequentially stacked on the semiconductor substrate;

forming a dielectric layer on the exposed portions of the first and second active regions and on the sidewalls of the first and second cell gates;

forming a first control line on at least a portion of each of the sidewalls of the first cell gate;

forming a second control line on at least a portion of each of the sidewalls of the second cell gate, wherein the second control line is parallel to the first control line; and

forming a data line perpendicular to the first and second control lines and connecting to the source regions of the first and second cell gates.

19. The method of Claim 18, further comprising forming a mask layer on the source region and then patterning the mask layer to form a mask pattern, and wherein the mask pattern is used as an etch mask in the patterning of the source region, the multiple tunnel junction barrier, the storage node and the gate dielectric region.

20. The method of Claim 18, further comprising:

forming a low-concentration impurity-doped region in the semiconductor substrate using the first and second cell gates as ion-implantation masks;

forming one or more spacers to cover at least a portion of the first and second sidewalls of the cell gates; and

forming a high-concentration impurity-doped region in the semiconductor substrate using the spacers and the first and second cell gates as ion-implantation masks.

21. The method of Claim 20, wherein the spacers are formed of polysilicon.

22. The method of Claim 18, wherein forming the first and second control lines comprises:

forming a conductive layer on at least portions of the dielectric layer;

patterning the conductive layer so that the conductive layer conformally covers the first and second cell gates;

forming an interlayer dielectric layer on the patterned conductive layer;

planarizing the interlayer dielectric layer and removing an upper part of the patterned conductive layer; and

removing a part of the patterned conductive layer to form the first and second control lines, wherein the first and second control lines have a height lower than the height of the source regions.

23. The method of Claim 18, wherein forming the first and second control lines comprises:

forming a conductive layer on at least portions of the dielectric layer;

patterning the conductive layer so that the conductive layer conformally covers the first and second cell gates;

forming a first interlayer dielectric layer on the patterned conductive layer;

etching the first interlayer dielectric layer so that the interlayer dielectric layer has a height lower than the top surface of the source regions; and

forming a second interlayer dielectric layer on the first interlayer dielectric layer.

24. The method of Claim 20, wherein forming the spacers comprises forming a spacer layer and then removing a part of the spacer layer that covers the source regions, and wherein a part of the conductive layer on the upper parts of the source regions is removed at the same time.

25. The method of Claim 22, wherein removing a part of the patterned conductive layer to form the first and second control lines comprises oxidizing a part of the patterned conductive layer.

26. The method of Claim 18, wherein forming the first and second control lines comprises:

forming a conductive layer on at least portions of the dielectric layer;

patterning the conductive layer so that the conductive layer conformally covers the first and second cell gates;

forming an interlayer dielectric layer on the patterned conductive layer;

planarizing the interlayer dielectric layer and removing an upper part of the patterned conductive layer; and

oxidizing a part of the patterned conductive layer to form the first and second control lines, wherein the first and second control lines have a height higher than the height of the source regions.

27. The method of Claim 18, wherein the first cell gate is formed so that a first part of the first cell gate is formed on the first field isolation layer and a second part of the first cell gate is formed on the second field isolation layer, and wherein the second cell gate is formed so that a first part of the second cell gate is formed on the second field isolation layer and a second part of the second cell gate is formed on the third field isolation layer.

28. The method of Claim 18, wherein the data line is formed after the first and second cell gates.

29. A method of fabricating a semiconductor device, comprising:

forming a plurality of field isolation layers on a semiconductor substrate having a cell array region and a peripheral circuit region to define a plurality of active regions;

forming a gate dielectric layer on the plurality of active regions;

sequentially forming a storage node layer, a multiple tunnel junction barrier layer, a source layer and a mask layer on the gate dielectric layer;

patterning the mask layer to form a mask pattern;

sequentially patterning the source layer, the multiple tunnel junction barrier layer, the storage node layer and the gate dielectric layer using the mask pattern as an etch mask to form a plurality of cell gates in the cell array region and a peripheral gate in the peripheral circuit region, the cell gates and the peripheral gate each having a gate dielectric region, a storage node, a multiple tunnel junction barrier and source region;

forming a dielectric layer covering the plurality of active regions and sidewalls of the cell gates and the peripheral gate;

forming a plurality of parallel control lines, wherein each control line is formed on a subset of the plurality of cell gates;

removing the mask pattern;

patterning the source region and the multiple tunnel junction barrier of the peripheral gate to form a peripheral gate contact hole;

forming a plurality of parallel data lines that are orthogonal to the plurality of control lines, wherein each data line is formed on a subset of the source regions of the cell gates;

forming a peripheral gate contact plug in the peripheral gate contact hole.

30. The method of Claim 29, before forming the control lines, further comprising:

forming a plurality of low-concentration impurity-doped regions in the semiconductor substrate using the cell gates and the peripheral gate as ion-implantation masks;

forming a plurality of spacers on sidewalls of the cell gates and the peripheral gate; and

forming a plurality of high-concentration impurity-doped regions in the semiconductor substrate using the spacers, the cell gates and the peripheral gate as ion-implantation masks.

31. The method of Claim 30, wherein the spacers comprise polysilicon spacers.

32. The method of Claim 29, wherein forming the plurality of control lines comprises:

forming a conductive layer on at least portions of the dielectric layer;

patterning the conductive layer using a photoresist pattern so that the conductive layer conformally covers the plurality of cell gates;

forming an interlayer dielectric layer on the patterned conductive layer;

planarizing the interlayer dielectric layer and removing an upper part of the patterned conductive layer to expose the mask pattern; and

removing a part of the patterned conductive layer to form the plurality of control lines, wherein the control lines have a height lower than the height of the source regions of the cell gates.

33. The method of Claim 32, wherein removing a part of the patterned conductive layer to form the plurality of control lines comprises oxidizing a part of the patterned conductive layer.

34. The method of Claim 32, further comprising:

performing an anisotropic etch process with respect to the first interlayer dielectric layer to form the first interlayer dielectric layer having a height lower than a bottom of the mask pattern; and

stacking and planarizing a second interlayer dielectric layer to expose the mask pattern.

35. The method of Claim 29, wherein the forming control lines comprises:

forming a conductive layer on at least portions of the dielectric layer;

patterning the conductive layer so that the conductive layer conformally covers the plurality of cell gates in the cell array region;

forming an interlayer dielectric layer on the patterned conductive layer;

planarizing the interlayer dielectric layer and removing an upper part of the patterned conductive layer to expose the mask pattern; and

oxidizing a part of the patterned conductive layer to form the plurality of control lines, wherein the control lines have a height higher than the height of the source regions of the cell gates.

36. The method of Claim 32, further comprising forming an insulation spacer covering sidewalls of the first interlayer dielectric layer and protruded upper sidewalls of the control lines after removing the mask pattern.

37. The method of Claim 36, wherein the insulation spacer is formed of one material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride and aluminum oxide.

38. The method of Claim 31, wherein the data lines and the peripheral gate contact plug are simultaneously formed.